Efficient, Linear Amplification of Varying-Envelope Signals Using FET's with Parabolic Transfer Characteristics

ADEL A. M. SALEH, SENIOR MEMBER, IEEE, AND M. F. WAZOWICZ

Abstract—**A linear, high-efficiency mode of operation is described for FET power amplifiers of varying envelope signals (e.g., single-sideband, quadrature-amplitude-modulation, and multicarrier signals). It makes use of FET's having parabolic transfer characteristics (PTC). It is shown theoretically and experimentally that the efficiency of the PTC mode is about 2 dB higher than that of the standard class-A mode. For example, two-tone, 4-GHz measurements on a Western Electric FET model 131-L showed that, for an output power of about 1.5 W and for a relative third-order intermodulation level of −35 dB, the power-added efficiency of the PTC mode was 20 percent, while that of the class-A mode was 13 percent. Comparisons are also made with other high-efficiency modes of operation proposed elsewhere.**

I. Introduction

TRADITIONALLY, satellite and terrestrial communications systems have utilized constant-envelope, single-carrier signals employing, for example, analog frequency modulation (FM), or digital phase-shift keying (PSK). The main advantage of such signals is their relative immunity to nonlinearities, which enables driving the transmitter power amplifier near saturation, thus maximizing its efficiency. However, these modulation schemes do not utilize the frequency spectrum efficiently. In fact, most communications systems that are being implemented today utilize analog, single-sideband (SSB) amplitude modulation [1]–[3] and digital, quadrature-amplitude-modulation (QAM) signals [4], which are both quite efficient in bandwidth utilization. Furthermore, it is often required to have a number of carriers share the same communications channel, e.g., a satellite transponder, in a frequency-division multiple-access (FDMA) mode of operation [5].

The problem with SSB, QAM, and FDMA signals is that they have highly time-varying envelopes, which require the power amplifier to operate with a high degree of linearity. This is accomplished by backing off the amplifier's output power away from saturation so as to restrict the range of signal envelope variations to the essentially linear region of amplification (see, for example, Fig. 1). In a field-effect-transistor (FET) power amplifier operating in standard class A, the required drain dc bias power is a constant that is set by the amplifier's saturated output power rating ($\alpha V_{o,\mathrm{sat}}^2$), and is essentially independent of the actual signal power level ($\alpha V_o^2(t)$). Thus, the amplifier efficiency is reduced from its maximum (single-carrier, near-saturation) value by the amount of the output power backoff. Such a reduction in efficiency results in a severe power penalty, which could be unacceptable, especially on a satellite where the available dc power is costly.

The operational efficiency of the amplifier can be greatly increased through the use of an analog [6],[7] or a digital [8] predistortion linearizer. Such a device, in effect, pushes the upper limit of the amplifier's linear region ($V_{o,\max}$) closer to saturation ($V_{o,\mathrm{sat}}$). However, even if this were done perfectly, the efficiency of the amplifier would still be reduced from its maximum value by an amount equal to the peak-to-average power ratio of the varying-envelope signal, which can be of the order of two to three decibels. A scheme, referred to as "class Ã," was proposed in [9], which eliminates most of this reduction. It involves the use of an external circuit to control dynamically the gate "dc" bias voltage of the FET with the envelope of the input RF signal such that the drain dc bias current is proportional to the envelope. Thus, the dc bias power would no longer be fixed at its maximum value (as is the case in standard class-A operation); rather, it would vary up and down with the signal envelope, thus reducing the dc power consumption and increasing the efficiency. As mentioned in [9], the use of this scheme is restricted to FET's with *linear transfer characteristics* (i.e., linear drain-current versus gate-voltage relationship for a fixed drain voltage) over most of their dynamic range. In fact, a linear transfer characteristic is implicit in standard class-A operation, and is usually sought by high-power FET device manufacturers.

In practice, the transfer characteristic of most FET's is nearly linear for high drain current, but tends to be parabolic near the pinchoff region. When operating in class A or Ã, one tries to avoid the parabolic region as much as possible. For some devices, e.g., the Western Electric high-power FET model 131-L, whose measured transfer characteristic is shown in Fig. 2, the parabolic region is quite pronounced. Actually, one can approximate this entire characteristic reasonably accurately with a single parabola.

Manuscript received July 13, 1984; revised March 29, 1985.

The authors are with AT&T Bell Laboratories, Crawford Hill Laboratory, Holmdel, NJ 07733.

0018-9480/85/0800-0703$01.00 ©1985 IEEE

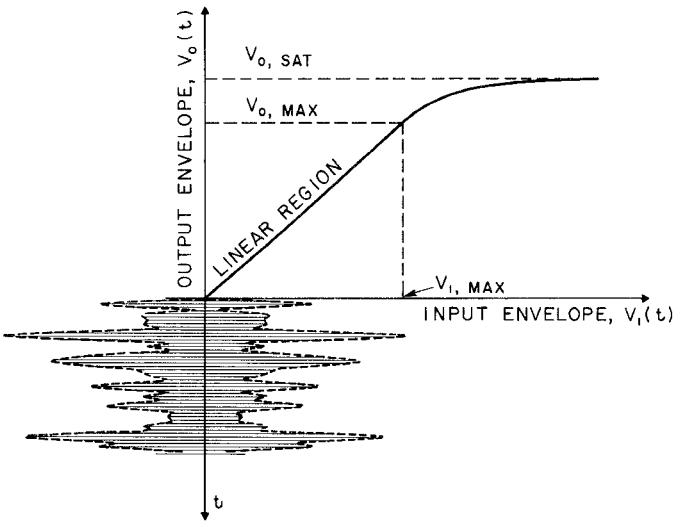


Fig. 1. Typical input–output RF envelope characteristic of an FET power amplifier, with a multicarrier input signal restricted to the linear range of amplification.

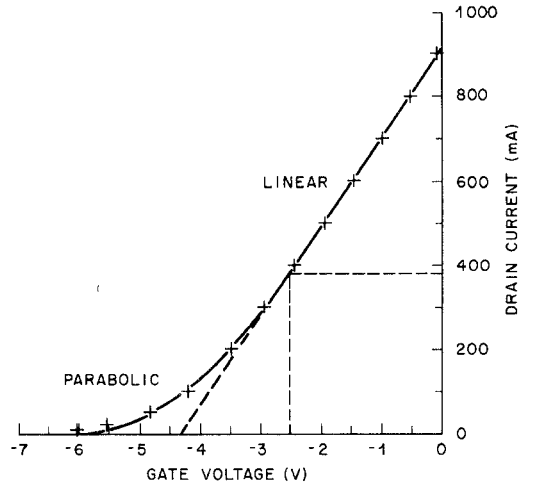


Fig. 2. The measured transfer characteristic of Western Electric high-power FET model 131-L for a drain voltage of 14 V.

In fact, Shockley's original theory on the FET [10], in which he employed a graded-channel model, predicts a very nearly parabolic transfer characteristic. This model is valid for FET's in which the ratio of gate length to channel thickness is large. It was later shown that, with this assumption, the transfer characteristic of the FET can be represented by a power-law having an exponent that is restricted to the remarkably narrow range between 2 and 2.25 for a broad range of channel doping profiles [11], [12, pp. 312–322]. On the other hand, if the channel is short, one can theoretically tailor the transfer characteristic to a wide variety of shapes, e.g., nearly linear or nearly parabolic, through the proper choice of the channel doping profile [13], [12, pp. 324–340].

In this paper, it is shown theoretically and experimentally that FET's with *parabolic transfer characteristics* (henceforth, PTC) are capable of linear amplification with approximately the same efficiency improvements of class A, but without the need for an external gate-bias-control

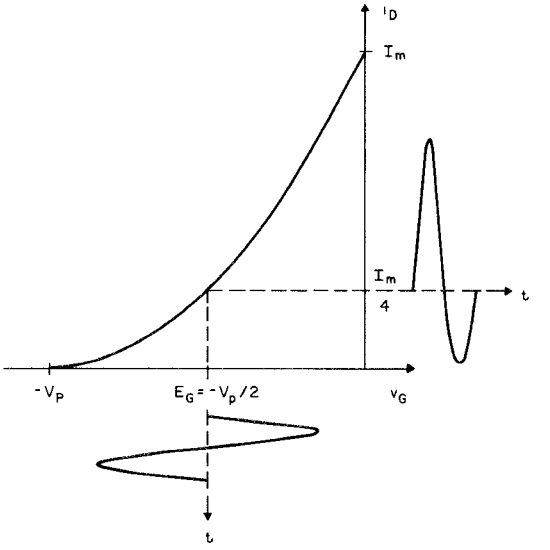


Fig. 3. Idealized operation in the PTC mode.

circuit. The dc drain current still follows the signal envelope, but this is done here automatically because of the parabolic characteristic. The circuit needed for the implementation of the PTC mode differs from that for standard class A in two very important aspects which, however, are minor in terms of cost and complexity. First, to avoid excessive intermodulation distortion, the drain dc bias circuit should have a provision to prevent the drain "dc" current variations from modulating the drain dc bias voltage. In most applications, this can simply be a shunt capacitor of a reasonable size. Secondly, to prevent premature saturation of the output power, the output RF tuning circuit should short circuit the second harmonic of the signal, which is generated by the parabolic characteristic.

II. Theory

A. Device and Circuit Models

Idealized models for the FET and the circuit are presented here, which are later employed to explain the theory of operation and to estimate the efficiency of the PTC mode of power amplification.

Let $i_D(t)$, $v_D(t)$, and $v_G(t)$ be the instantaneous drain current, drain voltage, and gate voltage, respectively. Furthermore, let I_m be the maximum allowable drain current, which is assumed to occur at $v_G = 0$; let V_m be the maximum allowable drain voltage, beyond which drain-to-gate breakdown would occur; and let V_P be the gate pinchoff voltage, at which $i_D = 0$. The transfer characteristic of the FET will be represented by the parabola

$$i_D = I_m(1 + v_G/V_P)^2 \tag{1}$$

which is depicted in Fig. 3. It will be assumed that (1) is valid, independently of v_D, provided that the operating range is confined to

$$0 \leqslant i_D \leqslant I_m \tag{2a}$$

$$0 \leqslant V_D \leqslant V_m \tag{2b}$$

$$-V_P \leqslant v_G \leqslant 0. \tag{2c}$$

The same terminology and assumptions, without the exponent in (1), were employed in the idealized FET model used in [9] for the analysis of classes A and Ã. This is done to facilitate direct comparison between these modes and the PTC mode.

A simplified circuit suitable for the PCT mode of power amplification is shown in Fig. 4. Conventional bias networks employing quarter-wave stubs and blocking capacitors are used for the gate and drain. A shunt capacitor C, which would not be needed in standard class-A operation, is included in the drain side to prevent bias current variations, which are induced by the signal envelope variations, from modulating the dc drain voltage. In the particular circuit of Fig. 4, that capacitor also presents a short circuit to the drain terminal at the second harmonic of the signal. This is done through the lower quarter-wave stub, which is a half-wave long at the second harmonic. In practice, the capacitor C would be a parallel combination of two capacitors, one for envelope frequencies, and the other for the second harmonic. The latter capacitor can also be replaced by an eighth-wave open-circuit stub.

B. Voltage and Current Waveforms

Let the band-limited input RF voltage be put in the general form

$$v_i(t) = V_i(t)\cos[\omega t + \phi(t)] \tag{3}$$

where $V_i(t)$ is the time-varying input envelope. Thus, the instantaneous gate voltage is

$$v_G(t) = E_G + v_i(t) \tag{4}$$

where E_G is the gate dc bias voltage, which is a negative quantity. Substituting (3) and (4) into (1) and expanding, one obtains the instantaneous drain current

$$\begin{aligned} i_D(t) = I_m\Big\{&[1+E_G/V_P]^2 + \tfrac{1}{2}[V_i(t)/V_P]^2 \\ &+ 2[1+E_G/V_P][V_i(t)/V_P]\cos[\omega t+\phi(t)] \\ &+ \tfrac{1}{2}[V_i(t)/V_p]^2\cos[2\omega t+2\phi(t)]\Big\}. \end{aligned} \tag{5}$$

The first line in (5) represents dc and low-frequency terms, the second line represents the fundamental output signal current, and the third line represents the second harmonic term. Because of the filtering properties of the output network in Fig. 4, only the fundamental component of the current would flow in the load R_L, resulting in an output signal voltage of the form

$$v_o(t) = V_o(t)\cos[\omega t + \phi(t)] \tag{6}$$

where

$$V_o(t) = 2(1+E_G/V_P)(I_m R_L/V_P)V_i(t) \tag{7}$$

is the output signal envelope.

The linear input–output relation indicated by comparing (3) to (6) and (7) should not be surprising. This follows since the only nonlinear distortions resulting from the parabolic characteristic of (1) are the low-frequency and the second-harmonic terms in (5), which are both easily filtered out (actually short circuited) by the output circuit, without affecting the signal. This would not have been possible if the input signal had an octave (or wider) bandwidth, since the spectra of both of the aforementioned nonlinear terms would fall within the signal bandwidth.

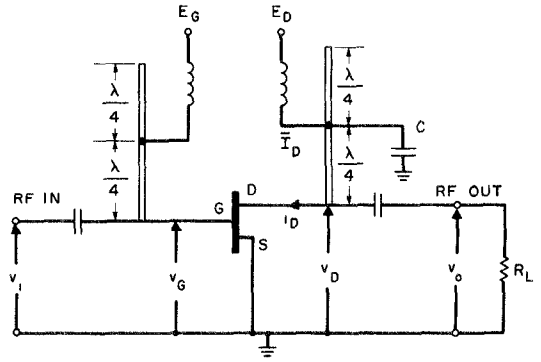


Fig. 4. Schematic circuit diagram showing the method of biasing the FET to enable operation in the PTC mode. The only difference between this and the standard class-A circuit is the capacitor C on the drain side, which is needed to prevent envelope-induced variations of the drain bias voltage, and to short circuit the second harmonic.

C. Optimizations and Normalizations

So far we have shown only that the PTC mode produces linear amplification. We now proceed towards finding its optimum output power and efficiency.

As depicted in Fig. 3, the gate should be biased at

$$E_G = -V_P/2 \tag{8}$$

in order to maximize the input envelope that can be handled by the amplifier without clipping, i.e., without violating (2c). This leads to

$$V_i(t) \leqslant V_{i,\max} \equiv V_P/2. \tag{9}$$

Similarly, in the output side, since $v_D(t) = E_D + v_o(t)$, it follows from (2b) and (6) that the output envelope limit is maximized if

$$E_D = V_m/2 \tag{10}$$

in which case

$$V_o(t) \leqslant V_{o,\max} \equiv V_m/2. \tag{11}$$

For optimum operation, $V_i(t)$ and $V_o(t)$ should attain their respective limiting values, $V_{i,\max}$ and $V_{o,\max}$, simultaneously. It can be seen from (7) that this is achieved when the load resistor assumes its optimum value

$$R_L = \frac{V_P V_{o,\max}}{I_m V_{i,\max}} = V_m/I_m. \tag{12}$$

Define the normalized signal envelope

$$r(t) \equiv \frac{V_o(t)}{V_{o,\max}} = \frac{V_i(t)}{V_{i,\max}} \leqslant 1 \tag{13}$$

where the second equality follows only if (12) is satisfied. Using (8), (9), and (13), one can put (5) in the normalized

form

$$i_D(t) = I_m\left\{\tfrac{1}{4} + \tfrac{1}{8}r^2(t) + \tfrac{1}{2}r(t)\cos[\omega t + \phi(t)] + \tfrac{1}{8}r^2(t)\cos[2\omega t + 2\phi(t)]\right\}. \quad (14)$$

D. Output Power and Drain Efficiency

The amplitude of the fundamental component of the output current is

$$I_o(t) = r(t)I_m/2 = V_o(t)/R_L \quad (15)$$

and, thus, the RF output power is

$$P_o(t) \equiv V_o(t)I_o(t)/2 = r^2(t)V_mI_m/8 \quad (16)$$

which is identical to that given in [9, eq. (9)] for classes A and Ã.

The "dc" drain bias current, which is time-dependent because of signal envelope variations, is given from (14) by

$$I_D(t) = [2 + r^2(t)]I_m/8. \quad (17)$$

Note that the drain bias current varies *linearly* with the signal power, starting from $I_m/4$ for no signal, i.e., $r^2(t) = 0$, to $3I_m/8$ for full signal drive, i.e., $r^2(t) = 1$. In class A, that current would have been fixed at $I_m/2$, independently of the signal level [9]. Of course, this is the main reason for the superiority of the efficiency of the PTC mode over that of class A.

The "dc" drain bias power is given, from (10) and (17), by

$$P_D(t) \equiv E_DI_D(t) = [2 + r^2(t)]V_mI_m/16. \quad (18)$$

The drain efficiency is defined by

$$\eta_D \equiv \bar{P}_o/\bar{P}_D \quad (19)$$

where the overbars indicate averaging over the signal envelope variations, i.e., over $r(t)$. Finally combining (19) with (16) and (18), one obtains the drain efficiency of the PTC mode of power amplification as

$$\eta_D = 2\overline{r^2}/(2 + \overline{r^2}). \quad (20)$$

The corresponding efficiencies of classes A and $\tilde{A}$ are given, from [9, eqs. (13a), (13b)], respectively, by

$$\eta_D^A = \overline{r^2}/2 \quad (21)$$

$$\eta_D^{\tilde{A}} = \overline{r^2}/2\bar{r}. \quad (22)$$

Note that for a fully driven constant-envelope signal, where $\overline{r^2} = \bar{r} = 1$, the drain efficiency for the PTC mode is 66.7 percent, while that for class A or Ã is 50 percent. However, the real advantage of the PTC mode, or, for that matter, class Ã, over standard class A is for varying-envelope signals. Table I gives a comparison of efficiencies among the three modes of operation for various signaling schemes. The signal statistics, i.e., the value of r^2 and $\bar{r}$ needed for the computation, were obtained from [9, table I]. In all cases in the table, with the exception of case 3, the signal envelope is assumed to lie entirely within the linear range of amplification, i.e., $\max[r(t)] = 1$. Rectangular pulses were assumed for digital signals, i.e., cases 4 through 8. In case 3, the signal is essentially Gaussian, and, hence, its envelope can theoretically go to infinity. Thus, as is explained in [9], the signal drive level is described by the *output power backoff* B_o. For the purpose of this paper, this is defined as

$$B_o = \frac{\text{maximum single-carrier linear output power}}{\text{average multicarrier output power}} = V_{o,\max}^2/\overline{V_o^2(t)} = 1/\overline{r^2} \geq 1. \quad (23)$$

For FET amplifiers, B_o is usually set within the range from 2 to 4 (i.e., 3 to 6 dB) for linear amplification of multicarrier signals.

It is clear from Table I that, for most signals, the theoretical drain efficiency of the PTC mode is about 50 percent, i.e., about 2 dB higher than that of standard class A, and is roughly equal to that of class Ã.

TABLE I
DRAIN EFFICIENCY OF CLASS-A, CLASS-Ã, AND PTC MODES FOR VARIOUS SIGNALING SCHEMES

Case	Signaling Scheme	Class A	Class Ã	PTC
1	One PM or FM Carrier	50.0%	50.0%	66.7%
2	Two Equal-Power PM or FM Carriers	25.0%	39.3%	40.0%
3	Large Number of PM or FM Carriers* (Also SSB and Gaussian Signals)	$\frac{1}{2B_o}$	$\frac{1}{\sqrt{\pi B_o}}$	$\frac{2}{B_o+2}$
4	16-QAM (4×4 Square Array)	27.8%	39.3%	43.5%
5	64-QAM (8×8 Square Array)	21.4%	34.9%	35.3%
6	256-QAM (16×16 Square Array)	18.9%	32.8%	31.8%
7	Infinitely Packed Square Array	16.7%	30.8%	28.6%
8	Infinitely Packed Disc	25.0%	37.5%	40.0%

See (23) for definition of B_o.

III. EXPERIMENT

An experimental 4-GHz FET power amplifier operating in the PTC mode is described in this section, and its performance is compared to that of the class-A mode. An ideal comparison would require a second FET that has a linear transfer characteristic, but is otherwise identical to the first FET. This, of course, is not a realistic requirement. Thus, it was decided to do the comparison using the same FET by biasing and tuning it differently for each mode of operation.

A. Device and Circuit

The device chosen was the Western Electric FET model 131-L, which has a 6-mm×1-μm gate. Such a device is

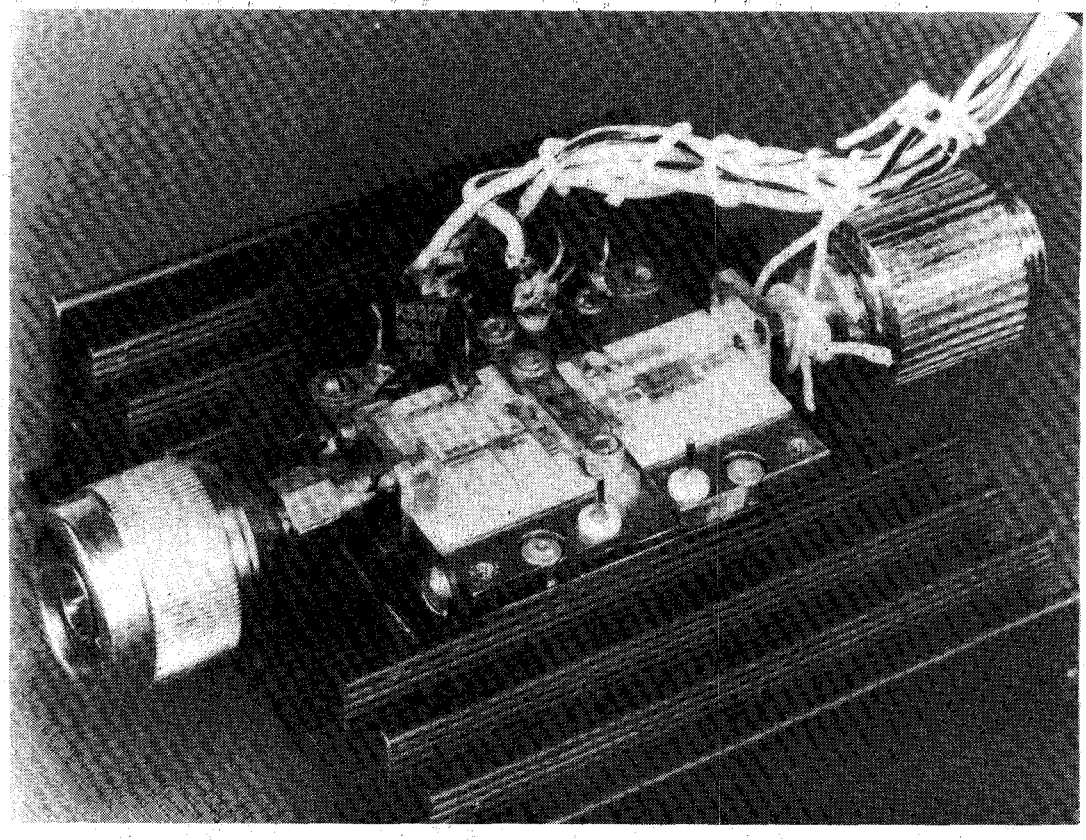


Fig. 5. A photograph of the amplifier under test, showing an 0.1-μF capacitor (#KS207/36-L1/105) mounted in the drain bias network.

quite suitable for two reasons. First, its transfer characteristic (see Fig. 2) has a pronounced parabolic region, which enables the PTC mode of operation. Secondly, this device was shown elsewhere [15] to give good efficiency and linearity when biased to operate in a standard class-A mode.

A photograph of the amplifier used for both modes is given in Fig. 5. The 131-L FET is shown in the middle of the figure, and is labeled by the number "27." The circuit is basically the same as the schematic of Fig. 4, except that the drain and gate sides are reversed. The capacitor C in Fig. 4 is implemented here by an 0.1-μF capacitor (which is labeled KS207/36L1/105 in Fig. 5) in parallel with a 30-pF chip capacitor (which is too small to see in Fig. 5). As mentioned earlier, the former capacitor is for short circuiting the envelope frequencies ($\approx$1.6 Ω at 1 MHz), and the latter for short circuiting the second harmonic ($\approx$ 0.7 Ω at 8 GHz).

The drain dc bias voltage for both modes was

$$E_D = 14 \text{ V}.$$

The gate dc bias voltages for the two modes were

$$E_G = -3.6 \text{ V (PTC mode)}$$

$$E_G = -2.0 \text{ V (class A)}.$$

A reference to Fig. 2 confirms that the former bias is within the parabolic region of the characteristic, and the latter is within the linear region.

The gold-on-alumina microstrip drain and gate circuits shown in Fig. 5 were earlier versions of those used in [15]. They were designed to provide the major part of the tuning of the FET for standard class-A operation over 400 MHz of bandwidth at 4 GHz. Additional tuning of the FET was done with the help of thin indium strips, which were affixed on the circuit by simply applying pressure with a teflon tool. The strips were easily trimmed, removed, and reapplied to provide the necessary tuning.

B. Experimental Setup and Tuning Process

A schematic diagram of the experimental setup is shown in Fig. 6. Two equal-level signals from two sweepers, operating around 4 GHz with a frequency separation from 1 to 30 MHz, were separately amplified then combined to deliver up to 0.5 W of two-tone power to the amplifier under test. The amplifier's input and output power levels were monitored with the help of two power meters connected via 10-dB directional couplers. A spectrum analyzer was also connected to the output coupler to measure the relative levels of the two-tone intermodulation products of various orders, i.e., third, fifth, etc. The drain and gate dc bias voltages and currents were all monitored. A large-signal, single-tone network analyzer, not shown in the figure, was used to provide the initial tuning through a swept measurement of S_{11} and S_{21}.

To make the final two-tone tuning process practical, the input power ($\overline{P}_i$), the output power ($\overline{P}_o$), and the drain dc

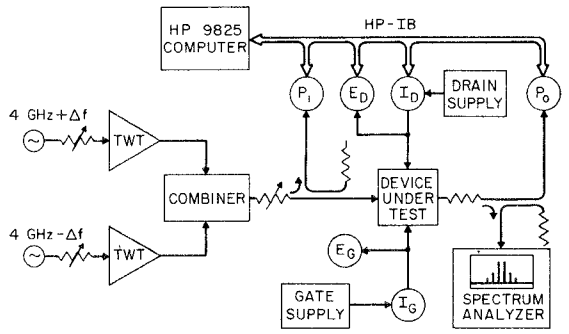


Fig. 6. Experimental schematic for the two-tone measurement.

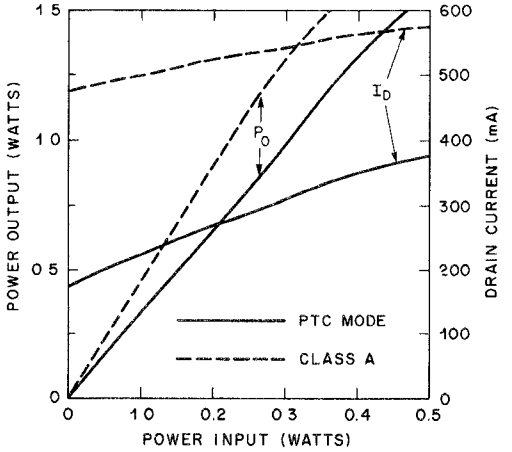


Fig. 7. Two-tone input–output power relations, and drain bias current versus input power curves for the two-tone PTC and class-A modes.

bias voltage (E_D) and current ($\bar{I}_D$) were all read by an HP-9825 computer via the HP-IB interface bus. The computer was used to calibrate the RF system, and to display directly $\bar{P}_t$ and $\bar{P}_o$ in watts, the gain

$$G \equiv \bar{P}_o/\bar{P}_t \tag{24}$$

converted to decibels, and the power-added efficiency

$$\eta_{\text{added}} \equiv (\bar{P}_o - \bar{P}_t)/\bar{P}_D = \eta_D(1-1/G) \tag{25}$$

where $\bar{P}_D$ is the drain dc bias power and η_D is the drain efficiency defined in (19). The power-added efficiency is, of course, a more meaningful quantity to maximize than the drain efficiency.

The value of η_{added} displayed by the computer and the level of the intermodulation distortion indicated by the spectrum analyzer were both observed during the cut-and-try tuning process described earlier. The object was to try to arrive at a compromise between maximizing the former and minimizing the latter. This was done by fixing the total two-tone input power level to 0.4 W, and trying to maximize η_{added}, while making sure that the largest intermodulation-product level, which was always that of the third order, remained below -35 dB. At the end of the tuning session, the operation bandwidth was checked. The whole process was redone if the ± 0.5-dB gain bandwidth was less than about 150 MHz. Raising the input power level beyond the aforementioned 0.4-W value resulted in a rapid increase in the intermodulation distortion, and in a dc gate current approaching $+10$ mA for class A, or -5 mA for the PTC mode. These positive and negative gate current levels were set by the device manufacturer as limits for reliable operation in a satellite environment.

C. Results

The measured, two-tone, 4-GHz (± 5 MHz), input–output power relationships are shown for class-A and the PTC modes in Fig. 7. The linear gain was 6.5 dB for the former mode, and 5.5 dB for the latter, up to an output power level of about 1.5 W. Shown on the same figure are plots of the corresponding drain dc bias currents versus input power. As predicted by (5) or (17), the current of the PTC mode increases almost linearly over nearly a 2-to-1 range as the input power increases from zero to its maximum

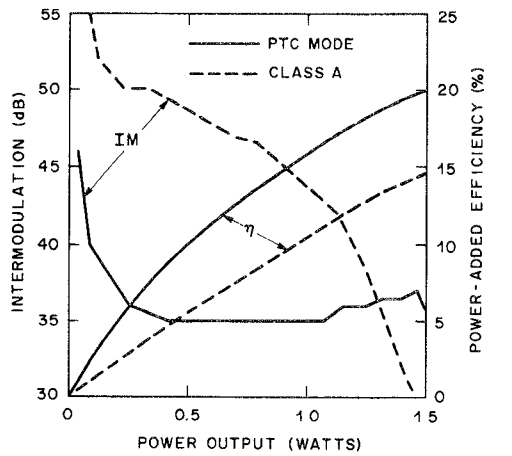


Fig. 8. Two-tone, third-order intermodulation distortions, and power-added efficiencies of the PTC and class-A modes as functions of the output power.

value. Actually, (17) predicts a current change over a 1.5-to-1 range. On the other hand, the class-A current varies only slightly with the input power, and is much higher than the PTC-mode current.

The final, and most significant, comparison between the two modes is given in Fig. 8, where the power-added efficiency and the two-tone, third-order intermodulation distortion for each mode are plotted against the output power. A comparison based on the same output power is more meaningful from a system standpoint than one based on the same input power. The functional shapes of the efficiency curves and the superiority of the PTC mode over class A are very close to the theory predicted by (20) and (21). Note that the power-added efficiencies given in Fig. 8 are under *linear* operating conditions.

The intermodulation performance shown in Fig. 8 indicates that the class-A mode is more linear than the PTC mode for output powers of less than about 1 W. However, for an intermodulation level of 35 dB, the PTC mode delivered 1.5 W at 20-percent power-added efficiency, while the class-A mode delivered about 1.4 W at only 13-percent

efficiency. Actually, the 35-dB intermodulation level is quite adequate for SSB and multicarrier operation.

The peculiar shape of the intermodulation curve for the PTC mode, i.e., being almost constant over a large range of the output power, is believed to occur because the nonlinear distortion results from the deviation of the transfer characteristic from an exact parabola. Such a behavior, for example, would result theoretically if this characteristic were made of two joined piece-wise parabolic parts. However, no further quantitive theoretical study of this point was made. It suffices here to conclude from the experiment that if more linear operation of the PTC mode is required, an FET with a purer parabolic characteristic would be needed.

The ± 0.5-dB bandwidth of the class-A mode was 220 MHz, while that of the PTC mode was 170 MHz. The efficiency and intermodulation distortion were relatively insensitive to the frequency separation between the two tones over a range from 1 to 30 MHz.

When the 0.1-μF capacitor in the drain bias circuit was removed, the performance of the class-A mode was not affected. However, the intermodulation distortion of the PTC mode was dramatically affected. For example, its value deteriorated by from 4 to 10 dB, and was sensitive to the frequency separation between the two tones. The intermodulation was highly correlated with the level of the envelope-induced variations of the drain bias voltage, which previously were suppressed by the 0.1-μF capacitor. When monitored on an oscilloscope, the drain voltage was seen to vary over a peak-to-peak value of up to several volts.

IV. Conclusions

It was shown theoretically and experimentally that FET's with parabolic transfer characteristics (PTC) are capable of efficient, linear power amplification of varying-envelope signals (e.g., SSB, QAM, and FDMA). The PTC mode offers about 2-dB increase in efficiency over the standard class-A mode (e.g., from 13 to 20 percent of power-added efficiency for a relative third-order intermodulation level of -35 dB). The efficiency is roughly equal to that estimated for the class-$\tilde{A}$ mode, which was proposed in [9] for efficient operation for FET's with linear transfer characteristics. However, the PTC mode does not require an external circuit for dynamically controlling the gate bias voltage as does the class $\tilde{A}$. The only circuit complexity needed for the implementation of the PTC mode over that needed for the standard class-A mode can be as simple as an added capacitor of a reasonable value (0.1 μF in the experiment).

It is appropriate at this point to mention class-B operation, which requires an FET with an essentially linear transfer characteristic. As shown in [9], that class of operation has a much higher *drain* efficiency than classes A and $\tilde{A}$, and also the PTC mode. In fact, the drain efficiency of class B, which is $\pi/2$ times that of class $\tilde{A}$ [9, eq. (13c)], is the highest possible efficiency for a *linear* amplifier. However, the amplifier's gain in class B is about 6 dB less than that in class A [9], [14]. This makes the *power-added* efficiency for class B inferior to the other classes, unless the amplifier's class-A gain is more than about 10 dB [9]. Since such a gain is not usually available for high-power FET's at higher microwave frequencies, class-B operation would actually be less efficient. Moreover, the gate voltage in class B is allowed to swing negatively beyond the pinchoff voltage, which may affect the reliability of the FET.

In conclusion, the PTC mode of power amplification presents itself as a practical means for very efficient operation of an FET amplifier. It is quite suitable for satellite applications where efficiency is of primary concern. For example, the 2-dB increase in efficiency predicted by the theory, and obtained experimentally, would result in about a 30-percent decrease in the required dc bias power on the satellite, or a 2-dB increase in the satellite's radiated RF power. Moreover, as discussed in the introduction, and as indicated by the experiment of Section III, manufacturing FET's with the desired parabolic characteristics does not seem to present a problem. A more purely parabolic characteristic would result in improved intermodulation performance.

Acknowledgment

The authors thank R. Trambarulo and R. D. Standley for providing the amplifier circuit.

References

[1] W. C. Jakes, Jr., Guest Ed., Special Issue on AR6A Single-Sideband Microwave Radio Systems, *Bell Syst. Tech. J.*, vol. 62, no. 10, pt. 3, Dec. 1983.

[2] R. J. Brown, Jr., M. L. Guha, R. A. Hedinger, and M. L. Hoover, "Compounded single sideband satellite transmission," in *IEEE Global Telecomm. Conf. Rec.* (GLOBCOM 1982), vol. 1, paper no. A5.4, Nov. 1982, pp. 146–150.

[3] K. Jonnalagadda, "Single sideband, amplitude modulated, satellite voice communication system having 6000 channels per transponder," *RCA Rev.*, vol. 43, pp. 464–488, Sept. 1982.

[4] J. C. Fuenzalida, D. Shimbo, and W. L. Cook, "Time-domain analysis of intermodulation effects caused by nonlinear devices," *COMSAT Tech. Rev.*, vol. 3, no. 1, pp. 89–143, Spring 1973.

[5] C. M. Thomas, M. Y. Weidner, and S. H. Durrani, "Digital amplitude-phase keying with M-ary alphabets," *IEEE Trans. Commun.*, vol. COM-22, pp. 168–180, Feb. 1974.

[6] A. A. M. Saleh, "Intermodulation analysis of FDMA satellite system employing compensated and uncompensated TWT's," *IEEE Trans. Commun.*, vol. COM-30, pp. 1233–1242, May 1982.

[7] R. P. Hecken, R. C. Heidt, and D. E. Sanford, "Predistortion for the TWTA," *Bell Syst. Tech. J.*, vol. 62, no. 10, pt. 3, pp. 3447–3464, Dec. 1983.

[8] A. A. M. Saleh and J. Salz, "Adaptive linearization of power amplifiers in digital radio systems," *Bell Syst. Tech. J.*, vol. 62, no. 4, pt. 1, pp. 1019–1033, Apr. 1983.

[9] A. A. M. Saleh and D. C. Cox, "Improving the power-added efficiency of FET amplifiers operating with varying-envelope signals," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-31, pp. 51–56, Jan. 1983.

[10] W. Shockley, "A unipolar 'field-effect' transistor," *Proc. IRE* (Transistor Issue), vol. 40, pp. 1365–1376, Nov. 1952.

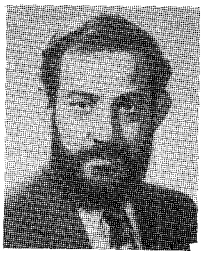
[11] R. D. Middlebrook and I. Richer, "Limits on the power-law exponent for field-effect transistor characteristics," *Solid-State Electron.*, vol. 6, no. 5, pp. 542–544, Sept.–Oct. 1963.

[12] S. M. Sze, *Physics of Semiconductor Devices*. New York: Wiley, 2nd ed., 1981, pp. 312–322.

[13] R. E. Williams and D. W. Shaw, "Graded channel FET's: Improve linearity and noise figure," *IEEE Trans. Electron. Devices*, vol. ED-25, pp. 600–605, June 1978.

[14] W. O. Schlosser and V. Sokolov, "Circuit aspects of power GaAs FET's," in *GaAs FET, Principles and Technology*, J. V. DiLorenzo and D. Khandelwal, Eds. Dedham, MA: Artech House, 1982, pp. 509–515.

[15] R. G. Gells, R. D. Standley, D. L. Wilson, and R. Trambarulo, "Highly linear, solid-state power amplifiers for single sideband via satellite applications," in *1983 IEEE MTT-S Int. Microwave Symp. Dig.*, paper no. T-3, June 1983, pp. 544–546.



Adel A. M. Saleh (M'70–SM'76) was born in Alexandria, Egypt, on July 8, 1942. He received the B.Sc. degree in electrical engineering from the University of Alexandria, Alexandria, Egypt, in 1963, and the M.S. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 1967 and 1970, respectively.

From 1963 to 1965, he worked as an Instructor at the University of Alexandria. In 1970, he joined AT&T Bell Laboratories, Holmdel, NJ, where he is engaged in research on microwave circuits, components, and communication systems.

Dr. Saleh is a member of Sigma XI.

Martin F. Wazowicz graduated from the RCA Institute in 1951, joined Western Electric in 1949, and AT&T Bell Laboratories in 1951. He worked on Mark IV and Essex Projects, *X*-band radio propagation experiments, mobile radio, satellite receivers, and investigations of various microwave components.